

Claims

- 1 1. A method for performing proximity effect correction on a layout of an integrated
2 circuit defined by a computer readable layout file, to produce a corrected layout file, the
3 method comprising:
4 receiving a polygon from the computer readable layout file, the polygon
5 corresponding to a portion of the integrated circuit;
6 performing using a data processor a fragmentation of the polygon into a set of
7 smaller shapes, based upon parameters of a manufacturing tool used for implementing the
8 layout;
9 performing using a data processor a proximity effect correction of at least one of
10 the smaller shapes in the set of smaller shapes to provide a computer readable corrected
11 layout file comprising a modified set of smaller shapes;
12 and
13 providing the computer readable corrected layout file to said manufacturing tool.
- 1 2. The method of claim 1, wherein the manufacturing tool comprises a mask writer.
- 1 3. The method of claim 1, wherein the manufacturing tool comprises a vector scan,
2 e-beam tool, and said parameters comprise scanning dimensions of said vector scan, e-
3 beam tool.
- 1 4. The method of claim 1, wherein one of said parameters is a minimum dimension
2 for the manufacturing tool, and the fragmentation is such that the smaller shapes do not
3 have a dimension smaller than said minimum dimension after said correction.
- 1 5. The method of claim 1, wherein one of said parameters is a maximum dimension
2 for the manufacturing tool, and the fragmentation is such that the smaller shapes do not
3 have a dimension larger than said maximum dimension after said correction.

- 1 6. The method of claim 1, wherein the corrected layout file is used to make a binary
2 mask.
- 1 7. The method of claim 1, wherein the corrected layout file is used to make an
2 attenuated phase-shifting mask.
- 1 8. The method of claim 1, wherein the corrected layout file is used to make a tri-tone
2 phase-shifting mask.
- 1 9. The method of claim 1, wherein the corrected layout file is used to make an
2 alternating aperture phase-shifting mask.
- 1 10. The method of claim 9, wherein two edges of one of the shapes in the set of
2 smaller shapes are adjacent to two distinct phase-shifting regions, the two phase-shifting
3 regions are substantially out of phase, and including storing information indicating that
4 said two edges of one of the shapes in the set of smaller shapes are adjacent to two
5 distinct phase-shifting regions.
- 1 11. The method of claim 10, wherein said information about the two edges is used to
2 facilitate the phase assignment of the phase-shifting regions.
- 1 12. The method of claim 1, wherein at least one edge of one shape abuts a boundary
2 of a critical area of the layout.
- 1 13. The method of claim 1, wherein the manufacturing tool comprises a mask
2 inspection tool.
- 1 14. The method of claim 1, wherein a boundary between adjacent shapes in the set of
2 smaller shapes is adjusted to account for a position of an edge of at least one of the
3 adjacent shapes which is modified by the proximity effect correction.

1 15. The method of claim 1, wherein a second polygon within proximity range of the
2 polygon is taken into account in the fragmentation of the shapes.

1 16. The method of claim 15, wherein a corner of the second polygon is used in the
2 fragmentation of the shapes.

1 17. A mask for defining a layer of material, said mask comprising:
2 a mask substrate;
3 a layout data file used to create a layout pattern on the mask substrate;
4 said layout pattern comprising material or physical shapes for transfer of an image
5 to a workpiece;
6 and said layout pattern having at least one shape having at least one segment
7 corrected for proximity effects, said such shape was defined before correction by
8 fragmenting a polygon of the layout data file, based upon parameters of a manufacturing
9 tool used for implementing the layout.

1 18. A method for manufacturing integrated circuits, said integrated circuits being
2 defined by a computer readable layout file, the method comprising:
3 receiving a polygon from the computer readable layout file, the polygon
4 corresponding to a portion of the integrated circuit;
5 performing using a data processor a fragmentation of the polygon into a set of
6 smaller shapes, based upon parameters of a manufacturing tool used for implementing the
7 layout;
8 performing using a data processor a proximity effect correction of at least one of
9 the smaller shapes in the set of smaller shapes to provide a computer readable corrected
10 layout file comprising a modified set of smaller shapes;
11 and
12 providing the computer readable corrected layout file to said manufacturing tool.
13 producing a mask having a mask layout based on the corrected layout file;
14 and
15 exposing a semiconductor treated with a material sensitive to radiation energy to
16 said radiation energy using said mask.

1 19. The method of claim 18, where the mask is produced using a vector-scan e-beam
2 tool by exposing a mask blank coated with an e-beam sensitive resist and said resist
3 polarity is chosen such that the shapes representing the critical dimensions of the layout
4 are exposed on the mask.

1 20. A method for producing a mask for a layer on an integrated circuit represented by
2 a computer readable layout file, comprising:
3 receiving a polygon from the computer readable layout file, the polygon
4 corresponding to a portion of the integrated circuit;
5 performing using a data processor a fragmentation of the polygon into a set of
6 smaller shapes, based upon parameters of a manufacturing tool used for implementing the
7 layout;
8 performing using a data processor a proximity effect correction of at least one of
9 the smaller shapes in the set of smaller shapes to provide a computer readable corrected
10 layout file comprising a modified set of smaller shapes;
11 and
12 producing a mask having a mask layout based on the corrected layout file.

1 21. A system for producing layout data, comprising:
2 a data processor which executes programs of instruction;
3 memory accessible by the data processor and storing programs of instruction, the
4 programs of instruction including logic to receive a polygon of a computer readable
5 layout file of a portion of the integrated circuit, performing using a data processor a
6 fragmentation of the polygon into a set of smaller shapes, based upon parameters of a
7 manufacturing tool used for implementing the layout, performing using a data processor a
8 proximity effect correction of at least one of the smaller shapes in the set of smaller
9 shapes to provide a computer readable corrected layout file comprising a modified set of
10 smaller shapes.

1 22. An article of manufacture, comprising a machine readable data storage medium
 2 storing programs of instruction, including logic to receive a polygon of a computer
 3 readable layout file of a portion of the integrated circuit, performing using a data
 4 processor a fragmentation of the polygon into a set of smaller shapes, based upon
 5 parameters of a manufacturing tool used for implementing the layout, performing using a
 6 data processor a proximity effect correction of at least one of the smaller shapes in the set
 7 of smaller shapes to provide a computer readable corrected layout file comprising a
 8 modified set of smaller shapes.

1 23. A method for performing proximity effect correction on a layout of an integrated
 2 circuit defined by a computer readable layout file, to produce a corrected layout file, the
 3 method comprising:
 4 receiving a polygon from the computer readable layout file, the polygon
 5 corresponding to a portion of the integrated circuit;
 6 performing using a data processor a fragmentation of at least one edge of the
 7 polygon into a set of segments, based upon parameters of a manufacturing tool used for
 8 implementing the layout;
 9 performing using a data processor a proximity effect correction of at least
 10 one of the segments in the set of segments to provide a computer readable corrected
 11 layout file;
 12 and
 13 providing the computer readable corrected layout file to said manufacturing
 14 tool.

1 24. A method for manufacturing integrated circuits, said integrated circuits being
 2 defined by a layout file, the method comprising:
 3 receiving a polygon from the computer readable layout file, the polygon
 4 corresponding to a portion of the integrated circuit;
 5 performing using a data processor a fragmentation of at least one edge of the
 6 polygon into a set of segments, based upon parameters of a manufacturing tool used for
 7 implementing the layout;

8 performing using a data processor a proximity effect correction of at least
9 one of the segments in the set of segments to provide a computer readable corrected
10 layout file;
11 producing a mask having a mask layout based on the corrected layout file;
12 and
13 exposing a semiconductor treated with a material sensitive to radiation energy to
14 said radiation energy using said mask.

1 25. The method of claim 24, where the mask is produced using a vector-scan e-beam
2 tool by exposing a mask blank coated with an e-beam sensitive resist and said resist
3 polarity is chosen such that the shapes representing the critical dimensions of the layout
4 are exposed on the mask.